Switched Capacitor Circuits
Introduction

• Until 1970’s analog signal processing used continuous time approach with resistors and capacitors.
• RC time constants can vary by as much as 20%.
• Capacitor ratios can be made accurate to about 0.1%.
• In addition to filtering, switched capacitor approach can be used for gain stages, VCO’s, modulators, DAC’s, etc.
Introduction

• A Switched Capacitor (SC) circuit is built of OPAMPs, switches, capacitors, and clocks.
• The OPAMPs used will have finite dc gain, finite unity gain frequency (GBW), slew rate, and dc offset.
• The capacitors are generally parallel plate capacitors and should be correctly modeled.
• The ON and OFF resistances and parasitic capacitances of the switches are important.
• The timing of the clocks is very important and non-overlapping clocks may be required.
Introduction
Introduction

• C1 is charged to V1 and V2 each clock period.
• The change in charge over one clock period \( \Delta Q_1 \) is given by,

\[ \Delta Q_1 = C_1(V_1 - V_2) \]

• Then,

\[ I_{avg} = \frac{C_1(V_1 - V_2)}{T} \]

\[ R_{eq} = \frac{T}{C_1} = \frac{1}{C_1f_s} \]
Technology

• Capacitors can be realized by four different techniques; metal-n⁺, metal poly, poly-poly, and metal-metal.
• Metal-n⁺ uses the gate oxide. Hence, large capacitance in a small area. However, voltage dependence and substrate noise.
• Metal-poly is more linear, but has large parasitics.
Technology

- Poly-poly is also quite good, but not available in many technologies. Also, large parasitic capacitances.
- MIM (Metal-Insulator-Metal) present only in modern technologies. Typically the best choice.
- You can even build your own vertical capacitors. However, matching will not be that good.
Technology

• In order to match capacitors, the Area/Perimeter ratios should be kept the same.
• Also, use symmetry and common centroid type layouts.
• Be careful about local and global type random errors.
Technology

\[ kohm = \frac{(v(3) - v(4))/i(v_{dum})}{V} \]
Technology

\[ \text{kohm} \quad \frac{(v(3) - v(4))}{i(vdum)} \]
Technology

kohm \[ \frac{(v(3) - v(4))}{i(v_{dum})} \]
Technology

- The first curve is the ON resistance of a single NMOS ($W=1\mu m, L=0.35\mu m$).
- The second curve is the ON resistance of a transmission gate with identical NMOS and PMOS devices.
- The final curve is the ON resistance of a transmission gate with a PMOS device of dimension $W=3.5\mu m, L=0.35\mu m$. 
Technology

• For small supply voltages, the two peaks come together and the resistance is not reduced properly.
• Now, let us decrease the supply voltage to 2.5V from 3.3V.
• Finally, we will decrease it to 0.8V.
• Take the most symmetric curve (with the larger PMOS device).
Technology

\[ kohm = \frac{v(3) - v(4)}{i(v_{dum})} \]
Technology

\[ \text{impedance} = \frac{(v(3) - v(4))}{i(vdum)} \]
Simple Calculations

• Let us now calculate the effect of \( R_{\text{ON}} \) on the operation of the circuit.

• The resistance creates a simple RC network with the capacitance of the SC circuit.

• One can easily write its behavior.

\[
\begin{align*}
V_{\text{out}} &= V_{\text{in}} \left(1 - \exp\left(-\frac{t}{RC}\right)\right) \\
\tau_s &= RC \ln\left(\frac{1}{\varepsilon}\right)
\end{align*}
\]
Simple Calculations

• From these expressions, one finds that for an error of less than 0.1%, $t_s$ should be chosen around 7RC.

• Using $R_{ON} = 10K$ and $C = 1\mu F$, $t_s = 70$ ns.

• Then, the clock period is 140 ns.

• This yields a max. clock frequency of 7 MHz.

• For larger clock speeds, either make the capacitances smaller, or the switches larger.
Simple Calculations

• The leakage currents through the OFF switches also dictate a minimum frequency.
• For our technology, this frequency is on the order of a few Hz at room temperature although it increases exponentially with temperature.
Simple Calculations

• Clock feedthrough is also important.
• The clock signals couple to the capacitors over the overlap capacitances.
• For $W = 3\, \mu m$ and $L = 0.7\, \mu m$, $C_{ov} = 1fF$.
• This creates about $3mV$ error in the stored voltage.
• Note however that this error is at the clock frequency and its harmonics.
Simple Calculations

• Charge redistribution is also important.
• The charge stored in the channel disappears when the transistor is switched OFF.
• For the same transistor, Q is about 6fC.
• If it divides into two equal portions (for source and drain), it creates 3mV error on the 1pF external capacitors.
Simple Calculations

• One solution to charge redistribution is to increase the capacitances. However, this will also increase the area and the power and decrease the speed.

• Another option is to insert a dummy switch of half size working at the opposite phase. This is successful if the charge is split into two equal portions.
Simple Calculations

Diagram with labels Phi1, Phi2, and other symbols.
Simple Calculations

- If the charge is not split equally, this might even make things worse.
- How the charge splits is a complex function of the rise and fall times of the clocks, the clock jitter, and the capacitances on each side of the switch.
- For steep rise and fall times, the capacitance ratios on either side have less effect.
Simple Calculations

• Another option to reduce the error is to use a fully differential approach.

• Also, using identical NMOS and PMOS devices helps.
Switched Capacitor Integrator

\[ v_o(n) = v_c(nT) \]

\[ v_c(t) \]

\[ v_c(t) \]

\[ v_c(t) \]

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\[ v_c(t) \]

\[ v_c(t) \]
Switched Capacitor Integrator

• Let $C_1 = aC$ and $C_2 = C$.
• Initially, ignore the $\phi_1$ switch at the output.
• Then, at phase 1,
  \[
  Q_{ac_1} = aCV_{in}(n - 1/2) \\
  Q_{c_1} = -CV_{out}(n - 1) \\
  V_{out}(n - 1/2) = V_{out}(n - 1)
  \]
• At phase 2,
  \[
  Q_{ac_2} = 0 \\
  Q_{c_2} = -CV_{out}(n)
  \]
Switched Capacitor Integrator

- Using charge conservation,
  \[ Q_{ac2} + Q_{c2} = Q_{ac1} + Q_{c1} \]
  \[ -CV_{out}(n) = aCV_{in}(n - 1/2) - CV_{out}(n - 1) \]

- This equation is valid if sampling is performed at \( \phi_2 \).
- If \( \phi_1 \) is preferred for sampling,
  \[ -CV_{out}(n) = aCV_{in}(n - 1) - CV_{out}(n - 1) \]
Switched Capacitor Integrator

• The first equation becomes in the z-domain

\[ CV_{out} = z^{-1}CV_{out} - z^{-1/2}aCV_{in} \]
\[ \frac{V_{out}}{V_{in}} = -a \frac{z^{-1/2}}{1 - z^{-1}} \]

• The second equation becomes

\[ CV_{out} = z^{-1}CV_{out} - z^{-1}aCV_{in} \]
\[ \frac{V_{out}}{V_{in}} = -a \frac{z^{-1}}{1 - z^{-1}} \]
Switched Capacitor Integrator

- The second equation looks like the better integrator. Let us now write the behavior of the first one in the continuous frequency domain.

\[ H(e^{j\omega T_c}) = -a \frac{e^{-j\omega T_c/2}}{1 - e^{-j\omega T_c}} = -a \frac{1}{e^{j\omega T_c/2} - e^{-j\omega T_c/2}} = -\frac{a}{j\omega T_c} \frac{\omega T_c/2}{\sin(\omega T_c/2)} \]

- For \( x = 0.1 \), \( \text{sinc}(x) = 0.997 \). For \( x = 0.05 \), \( \text{sinc}(x) = 0.999 \)
Switched Capacitor Integrator

• The second equation becomes in the frequency domain,

\[
\frac{V_{\text{out}}}{V_{\text{in}}} = -a \frac{\omega T_c/2}{j\omega T_c \sin(\omega T_c/2)} e^{-j\omega T_c/2}
\]

• This equation has a phase error in addition to the magnitude error.

• The phase error can create instabilities in higher order systems.
Switched Capacitor Integrator

• There are stray capacitances at the input. These are typically connected to ground. Hence they are shorted out.

• There are also stray capacitances also in the feedback.
  – If the stray capacitance is connected to the negative input of the OPAMP, it couples noise.
  – If it is connected to the output, it changes the load capacitance.
Switched Capacitor Integrator

• Moreover, the source and drain capacitances of the switches are added to the input capacitance, causing 5 - 10% error.

• Thus, this integrator is rarely used.

• Instead, a stray insensitive integrator should be preferred.
Switched Capacitor Integrator
Switched Capacitor Integrator

- Capacitor $C_1$ is now floating.
- Similar functions are carried out during the two phases.
- During phase 1, $C_1$ is charged to the input voltage.
- During phase 2, it is discharged to zero, forcing the charge to $C_2$. 
Switched Capacitor Integrator

\[ v_{c_1}(nT - T) \quad (a) \quad \quad v_{c_0}(nT - T) \quad (b) \quad \quad v_{c_0}(nT - T/2) \]
Switched Capacitor Integrator

• During phase 1 (figure a), the left side of the capacitor is charged positively. Its right side is negative.
• During phase 2 (figure b), it is applied to an inverting configuration.
• Therefore, the net result is that it is a non-inverting integrator.
Switched Capacitor Integrator

- Now, look at phase 1 (figure a) more closely.
- The stray capacitance to the left of $C_1$ is charged to the input voltage through a low impedance node.
- Thus, its charge does not affect the charge on $C_1$.
- The capacitance to the right is shorted to ground. Hence, no effect.
Switched Capacitor Integrator

• During phase 2 (figure b), the parasitic capacitor to the left of $C_1$ is shunted to ground.
• Its charge obtained during phase 1 disappears into ground.
• The parasitic capacitor on the right is now connected to the negative terminal of the OPAMP and hence to virtual ground.
• This way, one can choose the integrator capacitances smaller, saving power and speed.
Switched Capacitor Integrator
Switched Capacitor Integrator

\[
H(z) = \frac{C_1}{C_2} \frac{z^{-1}}{1 - z^{-1}}
\]

\[
H(z) = \frac{C_1}{C_2} \frac{z^{-1/2}}{1 - z^{-1}}
\]
Switched Capacitor OPAMP Requirements

• For a step input to an OPAMP with feedback factor $\alpha$, we expect the output to be independent of OPAMP gain and equal to $1/\alpha$.

\[
V_{out} = \frac{A_0 V_{step}}{1 + \alpha A_0}
\]

\[
\varepsilon = \frac{V_{step}/\alpha - V_{out}}{V_{step}/\alpha} = 1 - \frac{A_0 \alpha}{1 + \alpha A_0} \approx \frac{1}{\alpha A_0}
\]

\[
A_0 > \frac{1}{\alpha \varepsilon_{max}}
\]
Switched Capacitor OPAMP
Requirements

• For a maximum error of 0.05%, the required gain is 5000 – 10000.
• The settling time is also quite important.
• Let us call the error from the settling time the dynamic error $\varepsilon_D$.
• For a deviation of 0.1%, about 7 time constants are necessary.
• Let us look at this more analytically
Switched Capacitor OPAMP Requirements

• The dynamic error is given by,

\[ \varepsilon_D = \exp\left(-\frac{\alpha g_m t_s}{C_{L,ef}}\right) \]

\[ GBW = \frac{g_m}{2\pi C_{L,ef}} \]

\[ \varepsilon_D = \exp\left(-\alpha 2\pi GBW t_s\right) \]

\[ GBW = \frac{1}{\alpha 2\pi t_s} \ln\left(\frac{1}{\varepsilon_D}\right) = \frac{2f_c}{2\pi \alpha} \ln\left(\frac{1}{\varepsilon_D}\right) \]

\[ GBW > \frac{f_c}{\pi \alpha} \ln\left(\frac{1}{\varepsilon_D}\right) \]
Switched Capacitor OPAMP Requirements

• The term $\ln(1/\varepsilon_D)$ is about 7 for 0.1%, but 7.6 for 0.05%.

• For $\alpha$ unity, $2.4*f_c$ would be enough.

• Typically, large $a$ values are not present in switched capacitor circuits. Thus, the GBW is chosen about 3 times the clock period.
Switched Capacitor Noise

• Because the GBW is always larger than the clock frequency $f_c$, the noise is folded back towards the lowest frequency band. This is a heavy case of aliasing.

• We can write the total noise as

$$\overline{v_{ni}^2} = \frac{kT \ GBW}{C \ \frac{f_c}{2}}$$
Signal Flow Graph Analysis

• Take the following circuit as an example.
Signal Flow Graph Analysis

- The equivalent signal flow graph is

We can write the transfer function as

\[
V_o(z) = -\left(\frac{C_1}{C_A}\right)V_1(z) + \left(\frac{C_2}{C_A}\right)\left(\frac{z^{-1}}{1-z^{-1}}\right)V_2(z) - \left(\frac{C_3}{C_A}\right)\left(\frac{1}{1-z^{-1}}\right)V_3(z)
\]
Switched Capacitor Filters

- A first order active filter in continuous domain is as follows:
Switched Capacitor Filters

• A direct implementation of this is as follows:
Switched Capacitor Filters

• The transfer function of this filter is

\[ H(z) = -\frac{\left(\frac{C_1}{C_A}\right)(1-z^{-1}) + \left(\frac{C_2}{C_A}\right)}{1-z^{-1} + \frac{C_3}{C_A}} = -\frac{\left(\frac{C_1 + C_2}{C_A}\right)z + \frac{C_1}{C_A}}{\left(1 + \frac{C_3}{C_A}\right)z - 1} \]

• The poles and zeros are given by

\[ z_p = \frac{C_A}{C_A + C_3} \]
\[ z_z = \frac{C_1}{C_1 + C_2} \]
Switched Capacitor Filters

• For positive capacitance values, these are all between 0 and 1.

• However, in fully differential operation, it is easy to get a negative capacitance by interchanging the input wires.

• Then, setting $C_1 = -0.5C_2$, one can obtain a zero at $z=-1$. 
Switched Capacitor Filters

• Let us now carry out an exact analysis

\[
H(z) = -\frac{\left(\frac{C_1}{C_A}\right)\left(z^{1/2} - z^{-1/2}\right) + \left(\frac{C_2}{C_A}\right)z^{1/2}}{z^{1/2} - z^{-1/2} + \frac{C_3}{C_A}z^{1/2}}
\]

\[
H(e^{j\omega T}) = -\frac{j\left(\frac{2C_1 + C_2}{C_A}\right)\sin\left(\frac{\omega T}{2}\right) + \frac{C_2}{C_A}\cos\left(\frac{\omega T}{2}\right)}{j\left(2 + \frac{C_3}{C_A}\right)\sin\left(\frac{\omega T}{2}\right) + \frac{C_3}{C_A}\cos\left(\frac{\omega T}{2}\right)}
\]

• Making \(\omega T \ll 1\),

\[
H(e^{j\omega T}) \approx \frac{j \left(\frac{C_1 + C_2/2}{C_A}\right)\omega T + \frac{C_2}{C_A}}{j\left(1 + \frac{C_3}{2C_A}\right)\omega T + \frac{C_3}{C_A}}
\]
Switched Capacitor Filters

• This approximate equation will yield a zero and a pole at

\[ j\omega_z T = \frac{-C_2/C_1}{1+\frac{C_2}{2C_1}} \]

\[ j\omega_p T = \frac{-C_3/C_A}{1+\frac{C_3}{2C_A}} \]
Switched Capacitor Filters

• The direct implementation does not yield the best circuit.
• Some switches are unnecessary and could be shared with others.
Switched Capacitor Filters

- Switched capacitor filters should in general be implemented in a fully differential fashion.
Switched Capacitor Filters

• One can design more complex filters with the techniques shown above.
• Many higher order filters are designed with the SC technique nowadays.
• However, SC circuits have many more applications.
Differential SC Integrator

- Chart showing voltage (mV) over time (us)
  - Red line labeled v(10)
  - Green line labeled v(11)

- Voltage values: -600, -400, -200, 0, 200, 400, 600
- Time values: 0.0, 20.0, 40.0, 60.0, 80.0, 100.0
Differential SC Integrator

```
<table>
<thead>
<tr>
<th>Time (us)</th>
<th>Voltage (mV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.0</td>
<td>-60.0</td>
</tr>
<tr>
<td>2.0</td>
<td>-40.0</td>
</tr>
<tr>
<td>4.0</td>
<td>-20.0</td>
</tr>
<tr>
<td>6.0</td>
<td>0.0</td>
</tr>
<tr>
<td>8.0</td>
<td>20.0</td>
</tr>
<tr>
<td>10.0</td>
<td>40.0</td>
</tr>
</tbody>
</table>
```

Red line: \( v(10) \)
Green line: \( v(11) \)
Switched Capacitor Gain Circuits
Switched Capacitor Gain Circuits

- The following is a resettable gain circuit where OPAMP offset is cancelled.

\[ v_{\text{out}}(n) = -\left(\frac{C_1}{C_2}\right) v_{\text{in}}(n) \]
Switched Capacitor Gain Circuits

- During phase 2 (figure a), the OPAMP offset is stored on both $C_1$ and $C_2$. 
Switched Capacitor Gain Circuits

- At the end of phase 1 (figure b), the voltage across $C_1$ is given by $V_{C1}(n) = V_{in}(n) - V_{off}$.
- On the other hand, the voltage across $C2$ is given by $V_{C2}(n) = V_{out}(n) - V_{off}$.
- Then,
  $$\Delta Q_{C1} = C_1 \left[ V_{C1}(n) - (-V_{off}) \right] = C_1 V_{in}(n)$$
  $$V_{C2}(n) = V_{C2}(n - 1/2) - \frac{\Delta Q_{C2}}{C_2}$$
Switched Capacitor Gain Circuits

• Since the voltage across \( C_2 \) one period earlier was \(-V_{\text{off}}\) and \( \Delta Q_{C2} = \Delta Q_{C1} \),

\[
V_{C2}(n) = -V_{\text{off}} - \frac{C_1 V_{\text{in}}(n)}{C_2}
\]

• Finally, since one side of \( C_2 \) is connected to virtual ground which is at \( V_{\text{off}} \),

\[
V_{\text{out}}(n) = V_{\text{off}} + V_{C2}(n)
\]

\[
V_{\text{out}}(n) = V_{\text{off}} + \left( -V_{\text{off}} - \frac{C_1 V_{\text{in}}(n)}{C_2} \right) = -\left( \frac{C_1}{C_2} \right) V_{\text{in}}(n)
\]
Switched Capacitor Gain Circuits

• Note that offset cancellation is also good for combating 1/f noise.

• Also note that this structure requires a high slew rate from the OPAMP.

• A better structure is called the capacitive reset circuit and is as follows:
Switched Capacitor Gain Circuits

\[ v_{out}(n) = -\left(\frac{C_1}{C_2}\right) v_{in}(n) \]
Switched Capacitor Gain Circuits

• The main idea here is the inclusion of C3 which charges to the output voltage during phase 1.
• During phase 2, it prevents the output from going to zero. The output remains near the previous output level.
• Also, during phase 2, the charges of $C_1$ and $C_2$ are equal and thus $C_3$ does not effect the behavior of the circuit.